a ready queue including a ready queue link [having], the ready queue link comprising

a first information indicating [the] a first task control block for [the] a sequentially first task among tasks in the digital signal processor, and [the] a second task control block for [the] a sequentially last task among the tasks in the digital signal processor,

[and] a priority link group of priority links, [the] a number of [which is the same as the] the priority links being equal to a number of priority levels of the tasks in the digital signal processor, [having] and

a second information indicating [the] a third task control block for [the] a sequentially first task among tasks [of the] having same priority among the tasks in the digital signal processor, and [the] a fourth task control block for [the] a sequentially last task among the tasks having same priority;

and

an operating system for setting the first and second information according to [the] conditions of tasks for the digital signal processor, and controlling switching between the tasks of the ready queue.

2. (Amended) The real time control system of claim 1, wherein [each of] the first [and second] information [includes] comprises a first list pointer corresponding to

A1 Cncld.

the first task control block [of the first task] and a [last] second pointer corresponding to the second task control block [of the last task], and

the second information comprises a third list pointer corresponding to the third task control block and a fourth pointer corresponding to the fourth task control block.

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4. (Amended) The real time control system of claim 1, further comprising a waiting queue including a waiting queue link [including], the waiting queue link comprising

A2 Cmt

a third information indicating [the] a fifth task control block for the sequentially first task among the tasks in the digital signal processor, and [the] a sixth task control block for the sequentially last task among the tasks in the digital signal processor,

[and] a second priority link group of second priority links, [the] a number of [which is the same as] the second priority links being equal to the number of priority levels of the tasks in the digital signal processor, [having] and

a fourth information indicating [the] a seventh task control block for the sequentially first task among the tasks [of] having the same priority among the tasks in the digital signal processor, and [the] an eighth task control block for the sequentially last task among the tasks having the same priority,

wherein the operating system sets the third and fourth information so that resources for the tasks of the waiting queue are deterministically acquired.

5. (Amended) The real time control system of claim 4, wherein [each of] the third [and fourth] information [includes] comprises a fifth list pointer corresponding to the fifth task control block [of the first task] and a [last] sixth pointer corresponding to the sixth task control block [of the last task], and

the fourth information comprises a seventh list pointer corresponding to the seventh task control block and an eighth pointer corresponding to the eighth task control block.

A2 cm.+

6. (Amended) The real time control system of claim 1, wherein the operating system controls the ready queue so that switching between the tasks is achieved on [the] a basis of the priority link group, when task searching in the digital signal processor is based on an order of the priority [order] of the tasks, and

controls the ready queue so that switching between the tasks is achieved on [the] a basis of the ready queue link, when the task searching is based on a first-in first-out (FIFO) system.

7. (Amended) The real time control system of claim 1, further comprising a timer wheel for managing [the] timer control blocks for the tasks in a pointer arrangement structure, wherein the operating system inserts the timer control blocks

into corresponding slots of the timer wheel according to [the] a time set for the tasks in the digital signal processor.

8. (Amended) The real time control system of claim 7, wherein the timer wheel is divided into two timer wheels according to a predetermined reference time, and the operating system inserts timer control blocks corresponding to [the] slots of the first timer wheel when the time set for the tasks [are] is equal to or less than the predetermined reference time, and inserts timer control blocks corresponding to [the] slots of the second timer wheel when the time set for the tasks [are] is greater than the predetermined reference time and equal to or less than twice the predetermined reference time.

A2 Cont

9. (Amended) The real time control system of claim 8, wherein the operating system generates errors when the time set for the tasks [are] is greater than twice the predetermined reference time.

10. (Amended) The real time control system of claim 1, wherein a memory used to process the tasks in the digital signal processor is divided into an internal memory and an external memory in the digital signal processor, and the operating system manages the internal memory and the external memory using a memory